

Description

Drive circuit for a switch in a switching converter and method for driving a switch in a switching converter

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The present invention relates to a drive circuit for a switch in a switching converter and to a method for driving a switch in a switching converter, in particular in a step-up converter which converts a mains AC voltage into a DC voltage. Step-up converters of this type for converting a mains voltage into a controlled DC voltage are also referred to as power factor controllers (PFC).

10       Figure 1 shows a basic circuit diagram of such a PFC according to the prior art. The task of a PFC is to make available, from an input voltage  $V_{in}$ , a rectified, at least approximately load-independent output voltage  $V_{out}$  which serves for supplying a load, for example a DC-DC converter. The PFC comprises input terminals K10, K11, at which a mains AC voltage is present as input voltage  $V_{in}$ , the root-mean-square value of which may be between 90 V and 270 V in the case of a long-range power supply. The PFC comprises a bridge rectifier BG, and a further rectifier arrangement connected between the bridge rectifier BG and the output terminals K20, K21 and having a series circuit formed by a coil L and a diode D and a capacitor C connected between the output terminals K20, K21 and also having a semiconductor switch T, which is connected between a node that is common to the coil L and the diode D and the bridge rectifier BG and which serves to connect the coil in parallel with the output terminals of the bridge rectifier.

15       Figure 2 shows a basic circuit diagram of a drive circuit for the semiconductor switch T. The drive circuit has a clock input terminal K30 and a drive output terminal K31. The drive circuit also has a first input terminal K32 and a second input terminal K33. The first input terminal K32 is connected to a first node N1 which is connected to a first end of the coil L. The second input terminal K33 is connected to a second node N2 which is connected to a second end of the coil L. The drive output terminal K31 is connected to the semiconductor switch T.

20       The drive circuit also has a third input terminal K34 and a fourth input terminal K35. The third input terminal K34 is connected to a third node N3 which is connected to a first end of the diode D. The fourth input terminal K35 is connected to a fourth node N4 which is connected to a second end of the diode D. The drive circuit also has a fifth input terminal K36 and a sixth input terminal K37. The fifth input terminal K36 is connected to a fifth node N5 which is connected to a first end of the capacitor C. The sixth input terminal K37 is connected to a sixth node N6 which is connected to a second end of the capacitor C. The drive circuit also has a seventh input terminal K38 and an eighth input terminal K39. The seventh input terminal K38 is connected to a seventh node N7 which is connected to a first end of the semiconductor switch T. The eighth input terminal K39 is connected to an eighth node N8 which is connected to a second end of the semiconductor switch T.

25       The drive circuit also has a ninth input terminal K40 and a tenth input terminal K41. The ninth input terminal K40 is connected to a ninth node N9 which is connected to a first end of the diode D. The tenth input terminal K41 is connected to a tenth node N10 which is connected to a second end of the diode D. The drive circuit also has an eleventh input terminal K42 and a twelfth input terminal K43. The eleventh input terminal K42 is connected to an eleventh node N11 which is connected to a first end of the capacitor C. The twelfth input terminal K43 is connected to a twelfth node N12 which is connected to a second end of the capacitor C. The drive circuit also has a thirteenth input terminal K44 and a fourteenth input terminal K45. The thirteenth input terminal K44 is connected to a thirteenth node N13 which is connected to a first end of the semiconductor switch T. The fourteenth input terminal K45 is connected to a fourteenth node N14 which is connected to a second end of the semiconductor switch T.

30       The drive circuit also has a fifteenth input terminal K46 and a sixteenth input terminal K47. The fifteenth input terminal K46 is connected to a fifteenth node N15 which is connected to a first end of the diode D. The sixteenth input terminal K47 is connected to a sixteenth node N16 which is connected to a second end of the diode D. The drive circuit also has a seventeenth input terminal K48 and an eighteenth input terminal K49. The seventeenth input terminal K48 is connected to a seventeenth node N17 which is connected to a first end of the capacitor C. The eighteenth input terminal K49 is connected to an eighteenth node N18 which is connected to a second end of the capacitor C. The drive circuit also has a nineteenth input terminal K50 and a twentieth input terminal K51. The nineteenth input terminal K50 is connected to a nineteenth node N19 which is connected to a first end of the semiconductor switch T. The twentieth input terminal K51 is connected to a twentieth node N20 which is connected to a second end of the semiconductor switch T.

35       The drive circuit also has a twenty-first input terminal K52 and a twenty-second input terminal K53. The twenty-first input terminal K52 is connected to a twenty-first node N21 which is connected to a first end of the diode D. The twenty-second input terminal K53 is connected to a twenty-second node N22 which is connected to a second end of the diode D. The drive circuit also has a twenty-third input terminal K54 and a twenty-fourth input terminal K55. The twenty-third input terminal K54 is connected to a twenty-third node N23 which is connected to a first end of the capacitor C. The twenty-fourth input terminal K55 is connected to a twenty-fourth node N24 which is connected to a second end of the capacitor C. The drive circuit also has a twenty-fifth input terminal K56 and a twenty-sixth input terminal K57. The twenty-fifth input terminal K56 is connected to a twenty-fifth node N25 which is connected to a first end of the semiconductor switch T. The twenty-sixth input terminal K57 is connected to a twenty-sixth node N26 which is connected to a second end of the semiconductor switch T.

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The semiconductor switch T is driven in clocked fashion by a drive IC which, via the semiconductor switch T,

serves for controlling the power consumption of the PFC and thus for setting the output voltage  $V_{out}$ . For this purpose, a signal  $S_1$  dependent on the output voltage  $V_{out}$  is fed to the drive IC. During operation, the coil

- 5      L stores energy when switch T is closed and outputs said energy via the diode D to the output capacitor C and a connected load when switch T is subsequently open. In this case, the power consumption is dependent on the duty ratio of the switch T, that is to say on  
10     the ratio of switch-on duration to drive period. In this case, the drive period is usually prescribed by an oscillator signal generated in the drive circuit.

The duty ratio of the switch T varies over the period

- 15    of the usually sinusoidal input voltage, the frequency of which is significantly less than the switching frequency. This variation results from the fact that, in the case of a high instantaneous value of the input voltage, a shorter switch-on duration of the switch T  
20    suffices in order, per drive period for the maintenance of a required power consumption, to take up the same quantity of energy as in the case of a lower instantaneous value of the input voltage  $V_{in}$ . Overall, it holds true that as the root-mean-square value of the input  
25    voltage decreases, the duty ratio increases in order to achieve a given power consumption. The same holds true in the event of a rise in the power consumption of a load connected to the output terminals. In this case, too, the duty ratio of the switch increases in order to  
30    increase the power consumption overall for a given input voltage.

In the case of PFC with power consumptions above a legally prescribed limit value, there is the requirement

- 35    for a mains current consumption which is proportional to the input voltage. For a control of this type, a signal dependent on the input current is also fed to

the drive IC in accordance with figure 1. An example of a drive circuit for such a PFC is a module of the TDA 16888 type from Infineon Technologies AG, Munich.

5 During operation of a PFC, critical operating states may occur if, by way of example, the output voltage decreases to a value which lies outside the dimensioning limits of the switching converter. This is the case for example in the event of a mains failure or a so-called  
10 "brownout". "Brownout" denotes a disturbance in the supply mains in which the mains voltage falls, over a plurality of mains periods, below a limit specified for the power supply, said limit being 90 V, for example in the case of a long-range power supply.

15 The control of the PFC attempts to compensate for this decrease in the mains voltage by long switch-on periods of the switch T, in order to maintain a required power consumption. However, this can lead to impermissibly  
20 high currents in the switch T for which it is not designed. In order to avoid such high currents, PFCs with current limiting are known in which the switch T is switched off when its load current exceeds a maximum value. This has the effect that the switch T carries  
25 current only for in each case a short time, but the diode D carries current in each case for a correspondingly longer time, so that an impermissible heating of the diode D may result from this.

30 In order to avoid this problem, it is known to detect the root-mean-square value for the instantaneous value of the input voltage and to switch off the PFC if said root-mean-square value or the instantaneous value falls below a lower limit value. Such a PFC which detects the  
35 instantaneous value of the input voltage is disclosed for example in the data sheet UCC3817 from Uni-trode Inc. What is disadvantageous in this case is that

- detecting the input voltage requires a voltage divider which divides the input voltage down to values which can be processed by a logic circuit. The components required for the voltage divider increase the costs and
- 5 the circuitry outlay of such a PFC. Furthermore, detecting the root-mean-square value of the input voltage has the disadvantage that the input voltage has to be averaged over half a period of its temporal profile, which requires an integrator circuit having a large
- 10 time constant, which can only be realized by means of external components. However, such external components considerably increase the costs and realization outlay of such a circuit.
- 15 It is an aim of the present invention to provide a drive circuit for a switch in a switching converter, in particular in a PFC, which ensures a protection of the switching converter in the case of critical operating states, in particular in the case of a decrease in the
- 20 output voltage, and which does not require detection of the input voltage. Furthermore, an aim of the invention is a method for driving a switch in a switching converter, in particular in a PFC.
- 25 This aim is achieved by means of a drive circuit in accordance with the features of claim 1 and a method in accordance with the features of claim 15. The subclaims relate to advantageous refinements of the invention.
- 30 The invention's drive circuit for a switch connected to a rectifier arrangement in a switching converter which provides an output voltage from an input voltage comprises:
- 35 - a first input terminal for feeding in an output voltage signal dependent on an output voltage of the switching converter,

- a controller arrangement having at least one control amplifier and a compensation network having at least one capacitor, the output voltage signal being fed to said controller arrangement and the latter providing a control signal,
  - a protection circuit, which is designed to detect at least one critical state of the switching converter and which provides a protection signal in a manner dependent on the presence of a critical state, the protection circuit having a discharge circuit coupled to the compensation network,
- 15 15 - a signal generating circuit, to which the control signal and the protection signal are fed and which provides a drive signal having drive pulses according to the protection signal, the duty ratio of which drive signal is dependent on the control signal.
- 20 In the case of the switching converter according to the invention, the compensation network in the controller arrangement serves in a known manner for setting the control behavior of the overall arrangement, the at least one capacitor effecting an integrative portion of said control behavior. A control arrangement having a control amplifier and a compensation network can be gathered for example from the data sheet of the PFC module TDA4863 from Infineon Technologies AG. The charge stored in said at least one capacitor, or the voltage that can be tapped off across said capacitor, corresponds to an item of information about the average value of the previous profile of the output voltage and by way of that is indirectly related to the root-mean-square value of the input voltage, so that the control signal contains an item of information with regard to the root-mean-square value of the input volt-

age without the need for direct detection of the input voltage. The control amplifier forms a difference between the output voltage signal and a reference value and is coordinated with the compensation network for

5 example in such a way that the control signal rises in order thereby to lengthen the switch-on durations of the switch if the output voltage decreases in order thus to increase the power consumption and to counteract a further decrease in the output voltage.

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Besides an increased power consumption of the load, a decrease in the output voltage may also result from a decrease in the input voltage, both cases requiring an increase in the duty ratio of the switch in order, in 15 the first case, to increase the power consumption and, in the second case, to maintain a required power consumption with a reduced input voltage.

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The protection circuit serves for detecting at least one critical operating state, a first critical state being present for example when the output voltage has decreased below a lower limit value corresponding, for example, to 50% of the desired value of the output voltage. In the event of such a decrease in the output 25 voltage, it is assumed that the input voltage has decreased below a given lower limit value, which, for the reasons mentioned above, justifies switching off the switching converter for protection against damage.

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Switching off the switching converter owing to a great decrease in the output voltage is critical in the event of a reswitch-on for the following reason: if the output voltage decreases, then in the manner explained above, by means of the control signal at the output of 35 the controller arrangement, the duty ratio of the switch is firstly increased by means of the signal generating circuit in order to increase the power consump-

tion or to keep the power consumption constant in the event of a decreasing output voltage. Said control signal is preserved even after the switch-off owing to the integrating capacitor of the compensation network,

5 which, in the event of the switching converter being switched on again, may lead to damage when the input voltage is significantly greater after the reswitch-on than before the switch-off but the control signal initially effects a driving of the switch as in the case

10 of an input voltage that is small before the switch-off. If no current limiting is present, the initially long switch-on durations then lead to high input currents. If current limiting is present, then after said reswitch-on, as explained in the introduction in connection with figure 1, the result is short switch-on

15 durations of the semiconductor switch and long time durations during which the diode conducts current, which results in the diode being greatly heated. In order to avoid such problems in the event of the reswitch-on,

20 the protection circuit comprises the discharge circuit for the compensation network, said discharge circuit being designed to discharge the compensation network on detection of critical state which leads to a switch-off of the switching converter. Preferably, the discharge

25 circuit comprises a switch, which is connected between the compensation network and a reference-ground potential and which is driven in a manner dependent on a detection of a critical state by a control circuit.

30 Preferably, the discharge circuit detects the discharge state of the compensation network and generates a discharge signal dependent on the discharge state, a re-switch-on of the switching converter after a switch-off preferably being permitted again only when the compensation circuit has reached a predetermined discharge

35 state. This is preferably achieved by virtue of the fact that the protection signal is generated in a man-

ner dependent on the discharge signal and the switching converter remains switched off as long as the protection signal has a predetermined level.

- 5 In one embodiment, the discharge circuit has a current measuring arrangement for detecting a discharge current of the compensation network and generates the discharge signal in a manner dependent on an amplitude of the discharge current, for example by the discharge current being compared with a reference current.
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In order to enable the switching converter to start up, the protection circuit is preferably designed to detect the first critical state, in which the output voltage has decreased below a lower limit, only when the output voltage has previously exceeded an upper limit which indicates occasional normal operation.

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- 20 Besides the first critical state, the protection circuit may be designed to detect further critical states and to switch off the switching converter by means of the protection signal.

- 25 Thus, the protection circuit detects a second critical state for example when the output voltage, independently of the previous value therefore, lies below a limit value which is significantly less than the desired value of the output voltage and which indicates an interruption of the feedback loop which feeds the output voltage signal back to the drive circuit.
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- 35 A further critical state may be detected when an internal supply voltage of the drive circuit decreases below a value in the case of which a sufficient supply of the components of the drive circuit is not ensured.

One embodiment of the drive circuit according to the invention provides for the discharge circuit to be driven to discharge the compensation network upon detection of each of the critical states, while another

- 5 embodiment provides for the compensation network to be driven only upon detection of one or more selected critical states and, in the case of the remaining critical states, only to switch off the switching converter without discharging the compensation network.
- 10 The selected critical state in which the compensation network is discharged is, in particular, the state in which the output voltage decreases below the lower limit, since the abovementioned problems would otherwise occur during reswitch-on.

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A switch-off of the switching converter upon detection of a critical state is preferably effected by the interruption of a driving of the switch by the signal generating circuit according to the protection signal.

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The signal generating circuit may be a conventional signal generating circuit which provides a clocked drive signal for the switch in a manner dependent on an output-voltage-dependent control signal and a protection signal. In the case of a drive circuit for a PFC, a signal dependent on an input current may additionally be fed to said signal generating circuit in order to achieve a current consumption proportional to the input voltage. The signal generating circuit may additionally have protection mechanisms for protecting the circuit against an excessively high input current or for limiting the input current.

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The invention additionally relates to a method for driving a switch connected to a rectifier arrangement in a switching converter. This method comprises the provision of an output voltage signal dependent on an output voltage of the switching converter, the genera-

tion of a control signal from the output voltage signal by means of a control arrangement having a control amplifier and a compensation network having at least one capacitor, the provision of a drive signal having a sequence of drive pulses for the switch, the monitoring of at least one critical switching state of the switching converter, the interruption of the generation of drive pulses if a critical switching state is detected and at least partial discharge of the at least one capacitor of the compensation network.

In one embodiment, it is provided that a discharge current of the compensation network is detected and the compensation network is discharged until the discharge current has fallen below a predetermined threshold.

In one embodiment of the method, a first critical state is detected if the output voltage signal lies below a first threshold value, and is preferably detected only when the output voltage signal falls below the first threshold after the output voltage signal had previously exceeded a larger second threshold.

Preferably, a second critical state is detected if the output voltage signal falls below a third threshold, which is less than the first threshold. This state occurs for example in the event of an interruption in the feedback loop which feeds the output voltage back to the drive circuit.

In a further embodiment, a third critical state is detected if a supply potential of the drive circuit falls below a predetermined fourth threshold.

The present invention is explained in more detail below with reference to exemplary embodiments in the figures, in which

Figure 1 shows a basic circuit diagram of a PFC designed as a step-up converter according to the prior art,

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Figure 2 shows a switching converter designed as a step-up converter with a drive circuit according to the invention for a semiconductor switch in the switching converter, the drive circuit having a controller arrangement, a signal generating circuit and a protection circuit,

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Figure 3 shows a first exemplary embodiment of a protection circuit for a drive circuit according to the invention,

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Figure 4 shows a second exemplary embodiment of a protection circuit for a drive circuit according to the invention,

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Figure 5 shows a third exemplary embodiment of a protection circuit for a drive circuit according to the invention.

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In the figures, unless specified otherwise, identical reference symbols designate identical parts with the same meaning.

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In order to illustrate the construction and the functioning of a drive circuit according to the invention, figure 2 shows a switching converter designed as a step-up converter, the circuit topology of which corresponds to that of the switching converter already explained with reference to figure 1, with a drive circuit 100 according to the invention for a switch T designed as a MOSFET, which, in the case of the step-up

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converter, is connected in series with the coil L between the input terminals K10, K11 or between the output terminals of the bridge rectifier BG connected between the input terminals K10, K11. The task of the 5 drive circuit 100 is to drive the switch T in such a way that an at least approximately load-independent output voltage Vout is made available from an input voltage Vin which is present at the input and whose root-mean-square value may be subject to fluctuations.

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The drive circuit 100 has a first input terminal K1, to which is fed an output voltage signal S1 dependent on the output voltage Vout, which signal is generated from the output voltage Vout by means of a voltage divider 15 R10, R20 connected between the output terminals K20, K21. Said output voltage signal S1 is fed to a controller arrangement 40 having a control amplifier OTA1 and a compensation network 41, the controller arrangement 40 providing, from the output voltage signal 20 S1, a control signal S4 dependent on the output voltage, which control signal is fed to a drive signal generating circuit 20, which provides, at a connecting terminal K3 of the drive circuit 100, a drive signal S5 for the switch T in the switching converter. An input 25 current signal S2 dependent on an input current I of the switching converter is fed to the drive signal generating circuit 20 via a further input terminal K2, said input current signal being generated by means of a current measuring arrangement M10 connected into the 30 load circuit of the converter.

The drive signal generating circuit 20 comprises a pulse width modulator 21, to which the control signal S4 and the input current signal S2 are fed and which 35 provides a pulse-width-modulated signal S7, the duty ratio of which is dependent on the control signal S4 and the input current signal S2. The pulse width modu-

lator 21 may be a conventional pulse width modulator for use in switching converters which is designed to make available, from an output-voltage-dependent control signal S4 and an input current signal S2, a pulse-width-modulated signal for the driving of a switch T in a PFC, the pulse width modulator 21 generating the pulse-width-modulated signal preferably in such a way that the input current I of the switching converter is proportional to the voltage  $V_{in'}$  present at the output 10 of the bridge rectifier BG.

In the exemplary embodiment, the control amplifier OTA1 of the controller arrangement 50 is designed as a transconductance amplifier which supplies an output 15 current dependent on the difference between a reference signal V1 present at the input and the output voltage signal S1, the reference signal V1 multiplied by the value by which the voltage divider divides the output value  $V_{out}$  representing the desired value of the output 20 voltage  $V_{out}$ .

The compensation network 41, which, in the exemplary embodiment, comprises a parallel circuit formed by a capacitor C4 and a series circuit having a resistor R5 25 and a capacitor C5, is connected between the output of the control amplifier OTA1 and reference-ground potential GND, to which the input and output voltages  $V_{in}$ ,  $V_{out}$  and the rest of the signals are referred. In the exemplary embodiment, the control signal S4 is the 30 voltage across said compensation network 41 with respect to reference-ground potential. If the output voltage signal S1 is less than the reference signal V1 in the drive circuit illustrated, then the capacitors C4, C5 are charged further by means of the output current of the operational amplifier OTA1 and the control 35 signal S4 rises, in which case, by means of the drive signal generating circuit 20, with the control signal

S4 rising, the switch-on durations of the semiconductor switch T are lengthened in order to increase the power consumption of the switching converter and thus to counteract a further decrease in the output voltage

- 5 Vout. If the output voltage signal S1 exceeds the reference signal V1, then the capacitors C4, C5 are discharged via the operational amplifier OTA1, as a result of which the control signal S4 becomes smaller and the switch-on durations of the semiconductor switch T are  
10 reduced overall. As already explained, the switch-on durations, in the case of a sinusoidal input signal Vin, vary over the period of the input signal in order that the energy taken up per drive period of the switch T is kept constant, since a shorter switch-on duration  
15 is necessary in the case of a large instantaneous value of the input voltage Vin than in the case of a smaller instantaneous value of the input voltage Vin, in order to take up the same energy per switch-on period and thus to keep the power consumption approximately constant.  
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The drive circuit 100 furthermore comprises a protection circuit 30, which is designed to detect critical operating states of the switching converter and which  
25 generates a protection signal S3, which, depending on its level, prevents a driving of the semiconductor switch T and thereby switches off the switching converter.

- 30 In the exemplary embodiment, the pulse-width-modulated signal S7 generated by the pulse width modulator 21 and the protection signal S3 are fed to an AND element 22, downstream of whose output a driver circuit 23 is connected, at whose output the drive signal S5 is present.  
35 In this embodiment, a drive signal S5 having drive pulses is generated only when the protection signal S3 fed to an inverting input of the AND element 22 has a

low level. In this case, the pulse-width-modulated signal S6 is available unchanged at the output of the AND element 22. If the protection signal S3 has a high level, then the driving of the semiconductor switch T 5 is interrupted and the switch remains permanently open. In the exemplary embodiment, the switching converter is switched off by means of the protection signal S3, which serves as an enable signal for the drive signal generating circuit 20, and which enables the drive signal 10 generating circuit 20 in a manner dependent on said level for generating a drive signal S5 having drive pulses.

It goes without saying that any desired further circuitry realizations are conceivable in order to switch 15 off the switching converter according to the protection signal S3.

The protection circuit 30 comprises a detection circuit 31, which serves to detect critical operating states of 20 the switching converter and which provides the protection signal S3, and also a discharge circuit 32, which is driven by the protection signal S3 and is connected to the compensation network 41 and, in the example, is 25 designed to discharge the compensation network 41 according to the protection signal S3. The discharge of the compensation network upon detection of a critical operating state which leads to the switching converter being switched off by means of the protection signal S3 30 prevents the situation in which, in the event of a renewed reswitch-on after a noncritical operating state has been reached, a control signal S4 is present at the drive signal generating circuit 20, which control signal effects long switch-on durations of the semiconductor 35 switch T which, in the event of a large input voltage Vin, might lead to damage to the switching converter. This would be the case in particular if, due to

mains disturbances before the switch-off, the output voltage  $V_{out}$  decreased and the control signal  $S_4$  increased to high values in order to counteract a decrease in the output voltage  $V_{out}$ . Without the discharge circuit 32, this large control signal would still be present at the drive signal generating circuit 20 after the reswitch-on and initially bring about long switch-on durations, even if, in the meantime, the mains disturbances are no longer present and the input voltage  $V_{in}$  again assumes values which lie within the dimensioning range of the switching converter. If a current limiting function is realized, which limits the input current to a maximum value, then in the fault case explained, after the reswitch-on, the current limiting would be reached after a few "long" switch-on durations, this subsequently resulting in very short switch-on durations of the semiconductor switch and correspondingly long switch-on durations of the diode, which would damage the diode in the case of a full load current.

The discharge circuit 32 is preferably designed to detect the discharge state of the compensation network and to supply a discharge signal  $S_6$  back to the detection circuit 31, the detection circuit 31 generating the protection signal  $S_3$  in a manner dependent on said discharge signal  $S_6$  in order to enable the switching converter to be switched on again only when the compensation network 41 has reached a predetermined discharge state indicated by the discharge signal  $S_6$ .

The drive circuit is preferably integrated in a chip, in which case the compensation network 41 may be realized partly or completely with discrete components outside the chip.

Figure 3 shows an exemplary embodiment of a protection circuit 30 with a detection circuit 31 and a discharge circuit 32, the compensation network C4, C5, R5 also being illustrated for reasons of better understanding.

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In the exemplary embodiment, the output voltage signal S1 is fed to the detection circuit 31, the detection circuit 31, by means of a comparator K2, comparing the output voltage signal S1 with a reference signal V2 representing a lower limit value and setting an RS flip-flop RS1 if the output voltage signal S1 has decreased below the value of the reference signal V2. The protection signal S3 for inhibiting the switching converter is available at the output of the flip-flop RS1.

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In the exemplary embodiment, said protection signal S3 also serves for driving the discharge circuit 32, which, in the example, has a switch S32, which is connected between the compensation network 41 and reference-ground potential and which is driven by a logic circuit L32 in a manner dependent on the protection signal S3. In order to detect a discharge state of the compensation network 41, the discharge circuit 32 has a current measuring arrangement M32 in series with the switch S32, which outputs a current measurement signal to the logic circuit L32. The logic circuit L32 generates a discharge signal S6, which serves for resetting the flip-flop RS1, when a discharge current I32 has decreased below a predetermined value chosen such that, 15 when said discharge current is reached, the compensation network 41 is discharged to an extent such that the control signal S4 present at the latter has decreased to small values. The illustrated current measurement on the basis of the measuring arrangement M32 merely represents an example of the detection of the charge state of the compensation network 41. It goes without saying that it is also possible to use the 20 25 30 35

voltage across the compensation network or the charge stored in the network 41 to detect the state thereof.

Figure 4 shows a further exemplary embodiment of a protection circuit 30 with an example of a circuitry realization of the discharge circuit 32, the compensation network 41 also being illustrated in figure 4 for the sake of better understanding. In this example, a switch for discharging the compensation network is designed as a bipolar transistor N2, which is driven by the protection signal S3, the generation of the protection signal S3 also being explained below.

A resistor R4 is connected in series with the bipolar transistor N2. Moreover, a further bipolar transistor N1 is present in series with a further resistor R3, the resistance of which preferably corresponds to the value of the resistor R4, said further bipolar transistor N1 likewise being driven by the protection signal S3. The series circuit having the further bipolar transistor N1 and the resistor R3 is connected to a supply potential VCC via a control transistor N5 and a current mirror circuit P1, P2. The control transistor N5 is driven by an operational amplifier OPV, one of whose inputs is connected to the resistor R4 and whose other input is connected to the resistor R3 and which, given identical dimensioning of the resistors R3, R4 in the circuit branch with the bipolar transistor P2 of the current mirror, the control transistor N5, the resistor R3 and the transistor N1, brings about a current corresponding to the discharge current I32 of the compensation network 41. In a further branch of the current mirror, a reference current source Iq1 is connected in series with a current mirror transistor P1, an inverter INV being connected to a node common to the transistor P1 and the current source Iq1, the discharge signal S6 being present at the output of said inverter. If the dis-

charge current  $I_{32}$  is initially greater than the current supplied by the current source  $I_{q1}$ , then approximately the entire supply voltage  $VCC$  is dropped across the current source  $I_{q1}$ , so that the node common to the 5 transistor  $P1$  and the current source  $I_q$  is at a high potential. If the discharge current  $I_{32}$  falls below the reference current of the current source  $I_{q1}$ , then approximately the entire supply voltage  $VCC$  is dropped across the bipolar transistor  $P1$  and the potential at 10 the common node of the transistor  $P1$  and the current source  $I_{q1}$  decreases. The circuit illustrated thus serves as a comparator circuit for comparing the discharge current  $I_{32}$  with a reference current supplied by the current source  $I_{q1}$ , the discharge signal  $S6$ , via 15 the inverter, assuming a high level if the discharge current  $I_{32}$  is less than the reference current supplied by the current source  $I_{q1}$ .

As in the example in accordance with figure 3, the detection circuit 31 comprises a comparator  $K2$  for comparing the output voltage signal  $S1$  with a reference value  $V2$  representing a lower limit for the output voltage signal  $S1$ . In contrast to the example in accordance with figure 3, in the case of the exemplary embodiment in accordance with figure 4, the RS flip-flop  $RS1$  is set via the comparator  $K2$  not directly but via an AND element  $AND2$ , the output signal of the RS flip-flop  $RS1$  forming the protection signal  $S3$  via an OR element  $OR1$ . The AND element  $AND2$ , in conjunction with 25 a further comparator  $K3$  and also a further flip-flop  $RS3$ , has the effect that a protection signal  $S3$  is generated in the event of a decrease in the output voltage signal below the lower limit  $V2$  only when the switching converter was previously in a normal operating state in 30 which the output voltage signal  $S1$  was greater than an upper limit value  $V3$ . For this purpose, the output voltage signal  $S1$  is compared with the upper limit 35

value V3 by means of the further comparator K3, the flip-flop RS3 being set if the output voltage signal S3 exceeds the upper limit value V3. The output signal of the further flip-flop RS3 is fed to the AND element

- 5 AND2, it thereby being ensured that, in the event of a decrease in the output voltage S1 below the value of the lower limit value V2, the flip-flop RS3 can be set only when the further flip-flop RS1 has previously been set.

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The flip-flop RS1 is reset by the discharge signal S6 via a further AND element AND3, to which the output signal of the flip-flop RS1 is furthermore fed.

- 15 The further flip-flop RS3 is likewise reset via a further AND element AND1 by means of the output signal of the AND element AND2 and of the AND element AND3.

20 The arrangement with the two comparators K2, K3 and also the two flip-flops RS1, RS2 generates a state signal indicating a critical operating state at the output of the flip-flop RS1 only when the output voltage signal S1 has decreased below a lower limit value V2 after it had previously exceeded an upper limit value V3.

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In the exemplary embodiment, the detection circuit 31 detects a further critical operating state, which is determined by virtue of the fact that the output voltage signal S1 is less than a lower limit value V4, 30 which is preferably significantly less than the lower limit value V2. By way of example, the limit value V2 amounts to 50% of the desired value for the output voltage, while the limit value V4 serves for detecting an interruption in the feedback path which provides the 35 output voltage signal S1. The limit value V4 is therefore only slightly above reference-ground potential, by way of example. A further state signal is present at

the output of a comparator K4, which compares the output voltage signal S1 with the reference signal V4, the OR element OR1 combining the two state signals at the output of the comparator K4 and at the output of the flip-flop RS1 in order to make the protection signal S3 available therefrom.

By means of the signal S3, in the exemplary embodiment, the compensation network 41 is discharged both in the event of detection of the first critical operating state by the arrangement with the two comparators K2, K3 and the flip-flops RS1, RS3 and in the event of detection of the second critical operating state by the comparator K4 and the switching converter is switched off by means of the protection signal S3.

Figure 5 shows a further exemplary embodiment of a protection circuit, in which the discharge circuit 32 is driven only on detection of the first critical operating state, in order to discharge the compensation network 41, while upon detection of the second critical operating state, although a protection signal is generated, for switching off the switching converter, the discharge circuit is not driven.

In the case of the protection circuit illustrated in figure 5, a third critical operating state is detected by the supply potential VCC of the drive circuit being compared with a reference value V5 by a further comparator K5, a critical operating state being present when the supply potential VCC is less than the reference value V5, and the switching converter then being switched off by means of the protection signal S3. Upon detection of this third critical operating state, the discharge circuit 32 is not driven in the exemplary embodiment. In the example, the discharge circuit 32 is only driven by the output signal of the RS flip-flop

RS1 in a manner dependent on a detection of the first critical operating state.

Even though the drive circuit according to the invention and also the method for driving the switch in a switching converter have been illustrated on the basis of a PFC, it should be pointed out that the drive circuit and the drive method can be applied to any desired switching converters in which a controller arrangement having a control amplifier and a compensation network is present.

## List of reference symbols

K10, K11	Input terminals
K20, K21	Output terminals
Vin	Input voltage
Vout	Output voltage
L	Coil
T	Switch, MOSFET
D	Diode
C	Capacitor
I	Input current
Vin'	Rectified input voltage
Vcc	Supply potential
100	Drive circuit
K1, K2, K3	Connecting terminals
20	Drive signal, generating circuit
21	Pulse width modulator
22	AND element
23	Driver circuit
S7	Pulse-width-modulated signal
S3	Protection signal
S4	Output-voltage-dependent control signal
S2	Input current signal
S1	Output voltage signal
R10, R20	Voltage divider
V1	Reference signal
OTA1	Control amplifier
40	Control arrangement
41	Compensation network
C4, C5	Capacitors
R5	Resistor
30	Protection circuit
31	Detection circuit
32	Discharge circuit
S6	Discharge signal
RS1, RS3	RS flip-flops

AND1, AND2, AND3	AND elements
OR1	OR elements
K2, K3, K4	Comparators
V3, V4	Reference signals
P1, P2	pnp bipolar transistors
N1, N2, N5	npn bipolar transistors
OPV	Operational amplifier
I32	Discharge current
Iq1	Current source
INV	Inverter
L32	Drive logic
S32	Switch
M32	Current measuring arrangement